

FIG. 1A

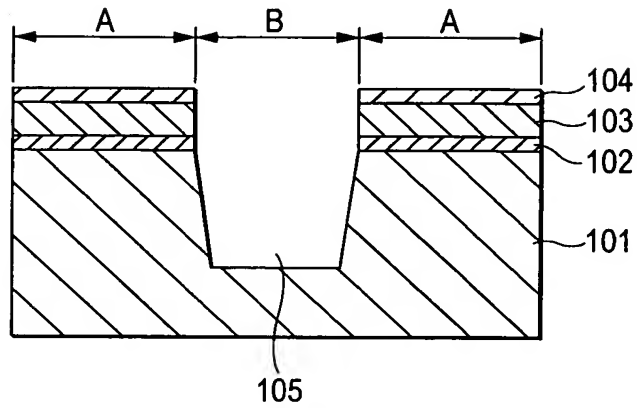


FIG. 1B

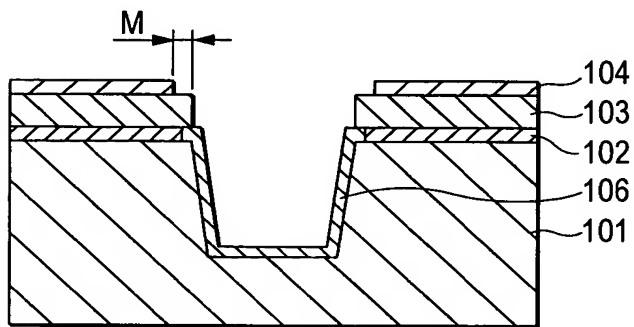
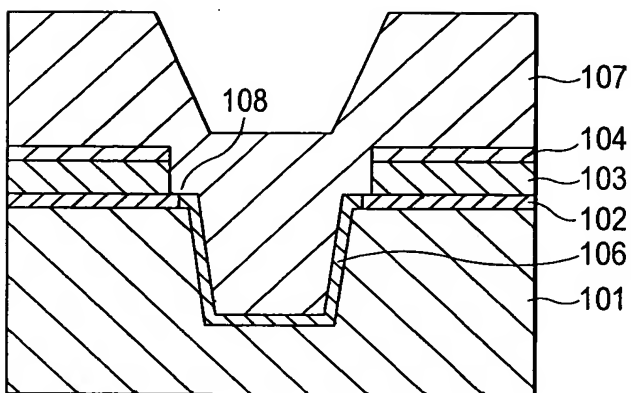


FIG. 1C



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FIG. 2D

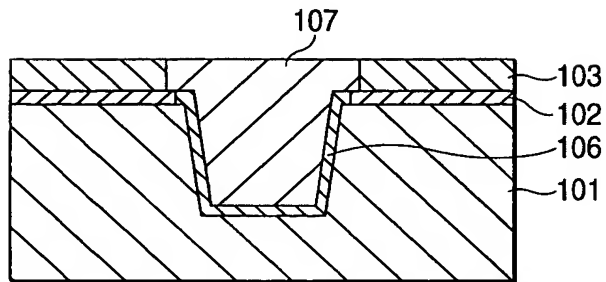


FIG. 2E

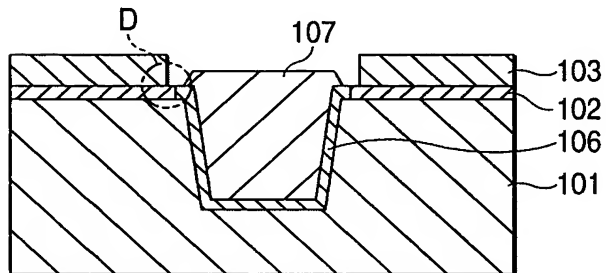


FIG. 2F

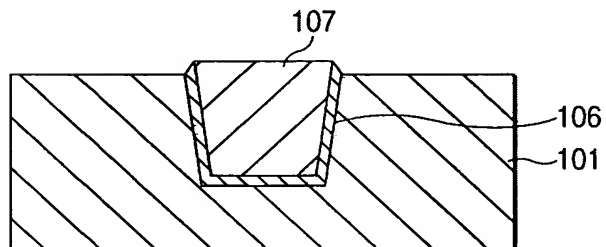


FIG. 3A

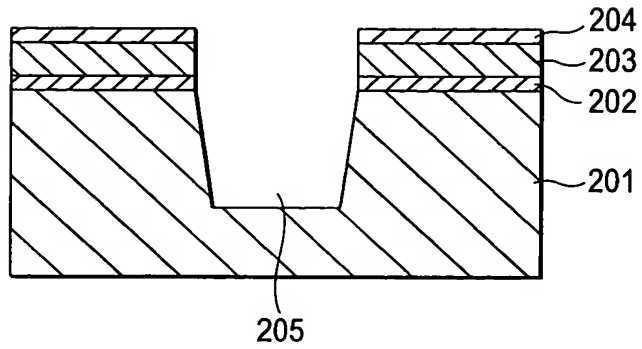


FIG. 3B

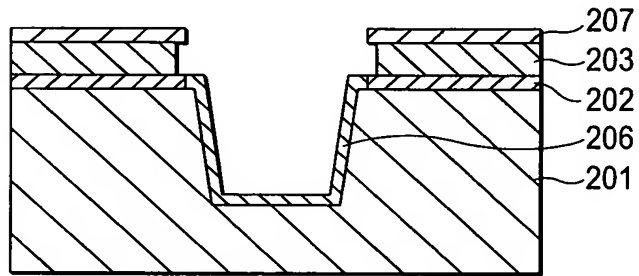
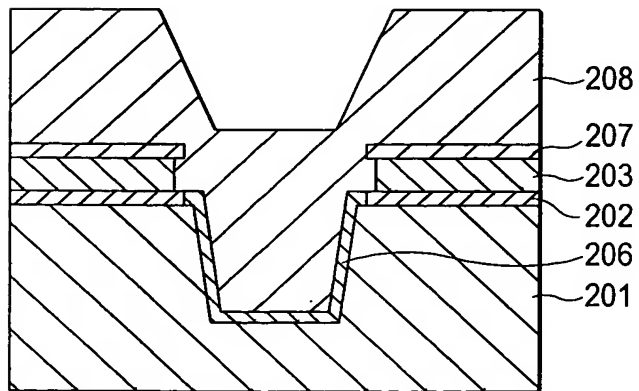


FIG. 3C



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FIG. 4D

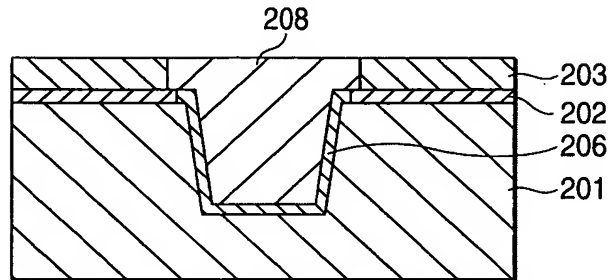


FIG. 4E

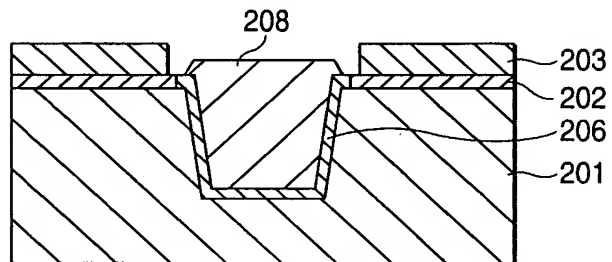
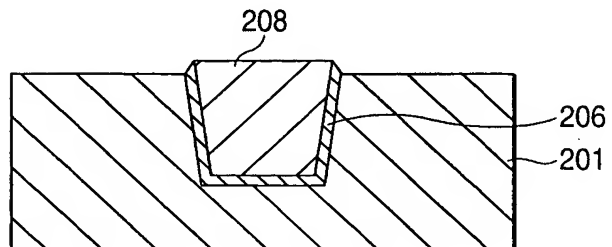


FIG. 4F



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Fig. 3 is a cross-sectional view of a semiconductor device. The device includes a substrate 301 with a trench 305. A first conductive layer 302 is formed on the bottom and side walls of the trench 305. A second conductive layer 303 is formed on top of the first conductive layer 302. A third conductive layer 304 is formed on top of the second conductive layer 303.

This cross-sectional view shows a trench structure within a substrate. The substrate is labeled 301 and contains a layer 306. Above the substrate is a series of layers: 302, 303, and 304. A trench is formed in the substrate, with its side walls labeled 308 and 309. The bottom of the trench is labeled 311. The top surface of the substrate is labeled 304.

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FIG. 6D

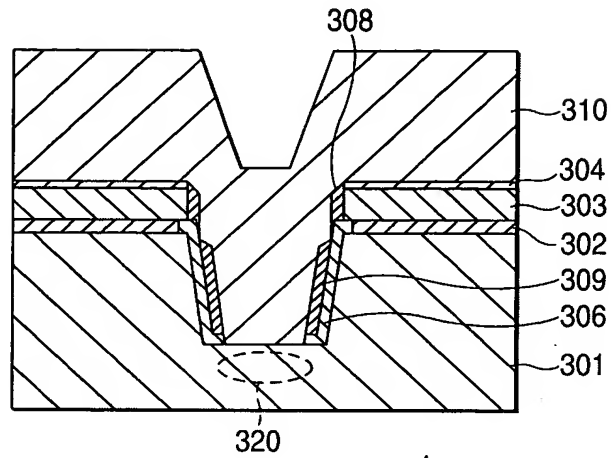


FIG. 6E

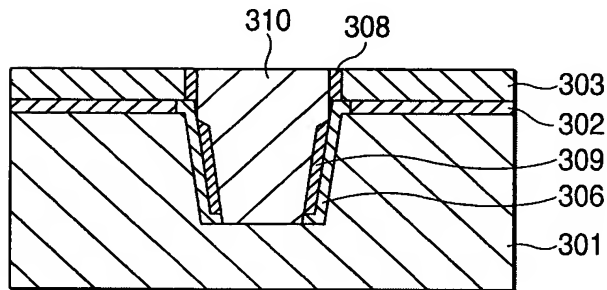
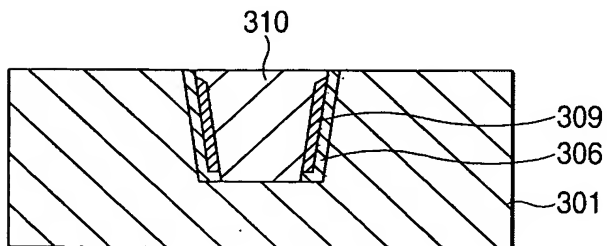


FIG. 6F



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FIG. 7A

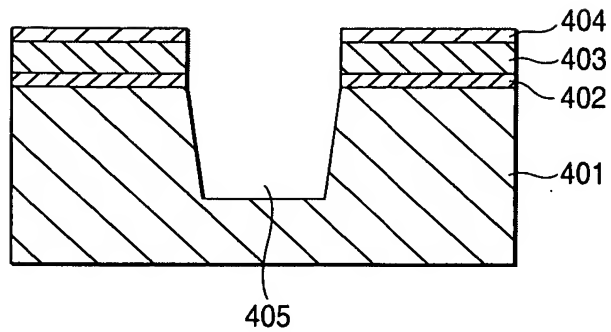


FIG. 7B

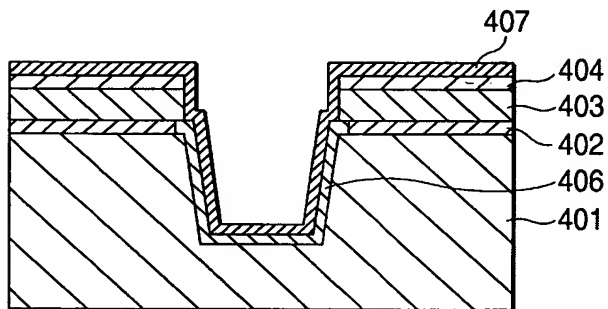
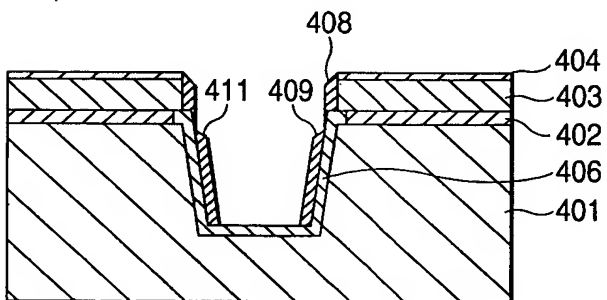


FIG. 7C



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FIG. 8D

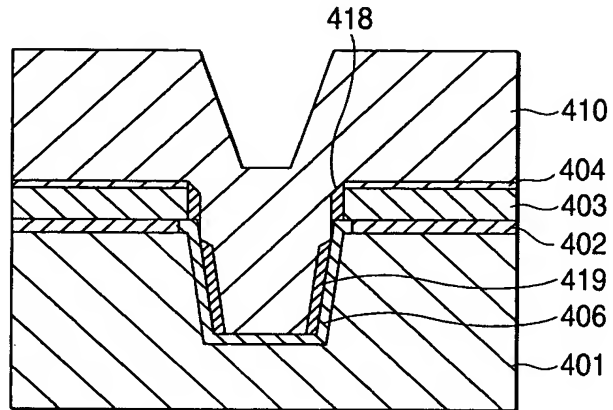


FIG. 8E

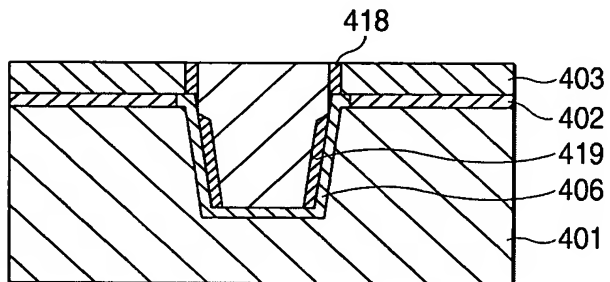
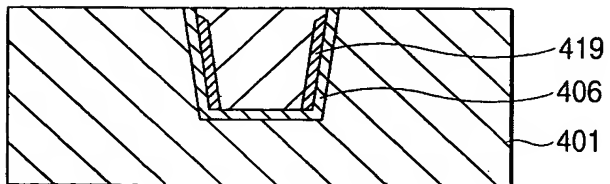
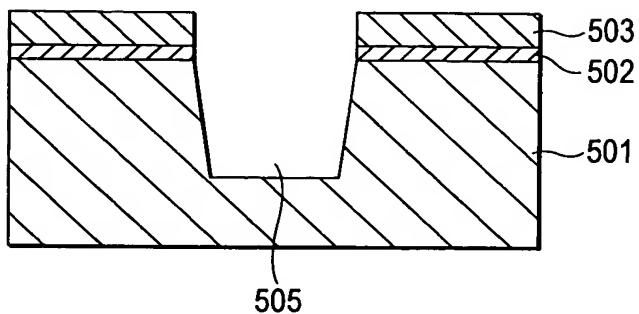


FIG. 8F

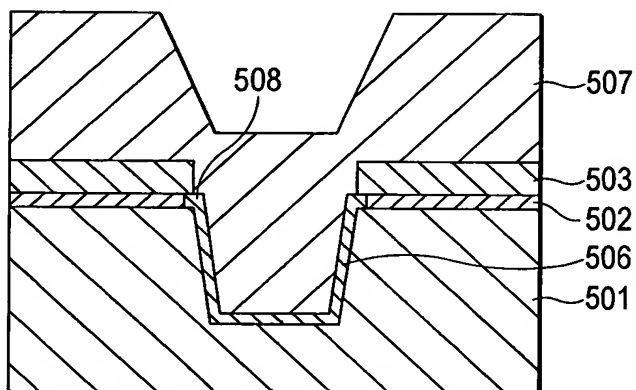




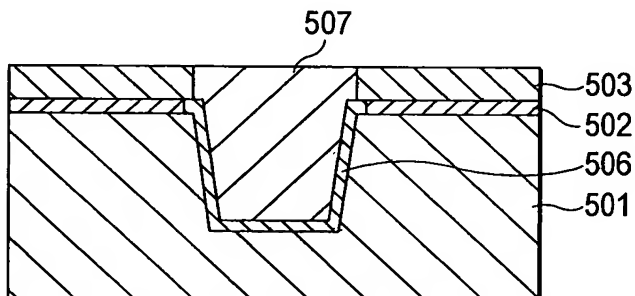
*FIG. 9A*  
*PRIOR ART*



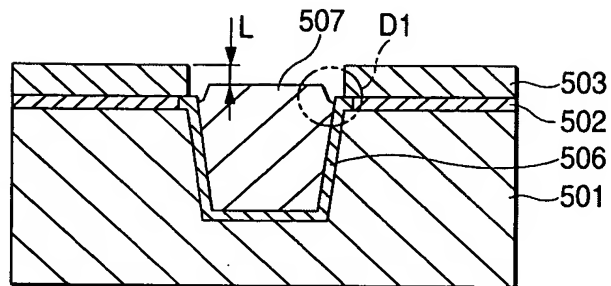
*FIG. 9B*  
*PRIOR ART*



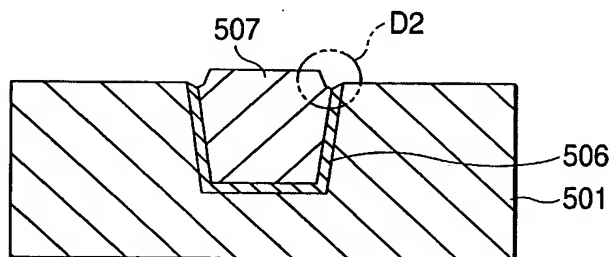
*FIG. 9C*  
*PRIOR ART*



**FIG. 10D**  
**PRIOR ART**



**FIG. 10E**  
**PRIOR ART**



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FIG. 11A  
PRIOR ART

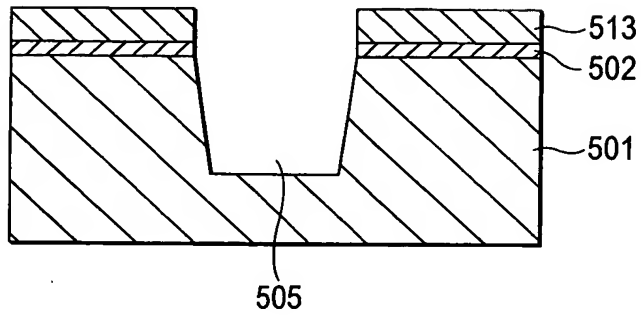


FIG. 11B  
PRIOR ART

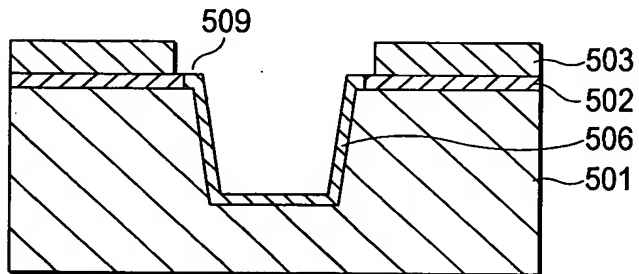
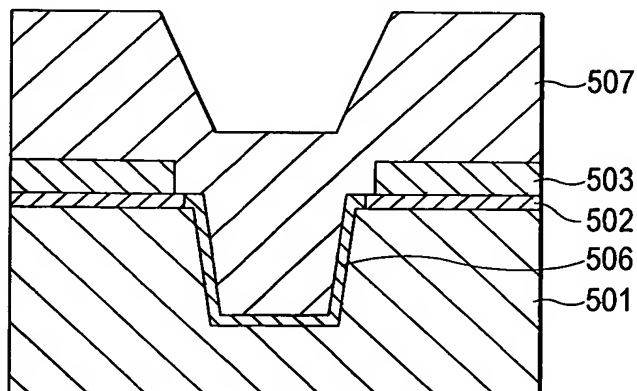
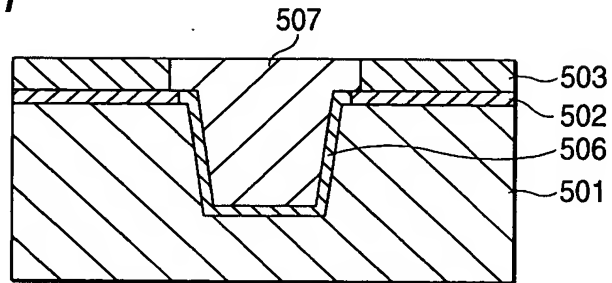


FIG. 11C  
PRIOR ART

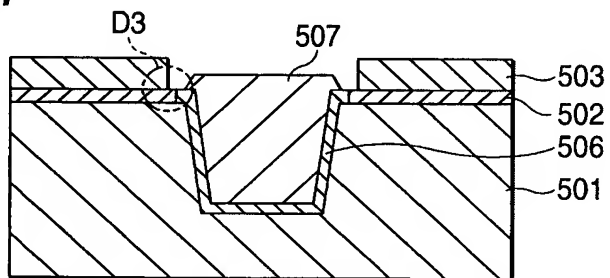


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*FIG. 12D*  
*PRIOR ART*



*FIG. 12E*  
*PRIOR ART*



*FIG. 12F*  
*PRIOR ART*

